CLAIMS

What is claimed is:

1. A method for designing an integrated circuit (IC), said method comprising:
compiling a hardware description language (HDL) code to produce a technology independent RTL (register transfer level) netlist;
allocating a portion of an area of said IC to a specific portion of said technology independent RTL netlist.

2. A method as in claim 1 wherein said allocating restricts circuitry created from said specific portion to said portion of said IC.

3. A method as in claim 1 further comprising:
mapping said technology independent RTL netlist to a selected technology architecture.

4. A method as in claim 3 wherein said IC comprises one of a programmable logic device or an Application Specific IC (ASIC).

5. A method as in claim 3 wherein said mapping is performed after said allocating.

6. A method as in claim 3 further comprising:

performing a place and route operation after said mapping to implement said IC in said selected technology architecture.

7. A method as in claim 3 further comprising:
optimizing a design of said IC after said allocating.

8. A method as in claim 7 wherein said optimizing optimizes said IC by removing duplicative logic or input/outputs.

10 ~~9~~. A method as in claim 3 wherein said HDL code is created without regard to said allocating.

9 ~~10~~. A method as in claim 7 wherein said optimizing and said mapping are performed after said allocating.

11. A method as in claim 3 further comprising:
mapping portions of said technology independent RTL netlist to a selected technology architecture wherein estimates of IC resources are obtained from said mapping portions and wherein said mapping portions is performed after said compiling and before said mapping.

13 ~~12~~. A method as in claim 3 further comprising:

optimizing interconnects between modules of said technology independent RTL netlist before said allocating.

12. ~~13.~~ A method as in claim 11 wherein said estimates are used to decide how to perform said allocating.

14. A method as in claim 12 wherein a user considers said estimates and selects a command to decide how to perform said allocating.

15. A method as in claim 3 wherein said IC comprises a programmable logic device and wherein said method further comprises:

testing a prototype of a system with said IC;

performing a synthesis of said HDL code to generate at least one Application Specific Integrated Circuit (ASIC).

16. A method as in claim 3 further comprising:

partitioning said technology independent RTL netlist between representations of said IC and another IC.

17. A method as in claim 16 wherein said partitioning is performed before said mapping.

18. A method as in claim 16 further comprising:

selecting logic designed for placement on one of said IC and said another IC and replicating said logic for placement on the other of said IC and said another IC.

19. A method as in claim 16 further comprising:

selecting one RTL component in said technology independent RTL netlist and splitting said one RTL component into a first RTL component designed for placement on said IC and a second RTL component designed for placement on said another IC.

23. ~~20.~~ A digital processing system for use in designing an integrated circuit (IC), said digital processing system comprising:

a display device;

a memory;

a processor coupled to said memory and to said display device, said processor allocating a specific portion of a technology independent RTL (register transfer level) netlist to a portion of said IC, said technology independent RTL netlist being stored in said memory.

24. ~~21.~~ A digital processing system as in claim ~~20~~ 23 wherein said processor compiles a hardware description language (HDL) code to produce said technology independent RTL netlist and wherein said allocating restricts circuitry created from said specific portion to said portion of said IC.

25. ~~22.~~ A digital processing system as in claim ~~21~~ 24 wherein said IC comprises one of a programmable logic device or an ASIC.

26. ~~23.~~ A digital processing system as in claim ~~21~~ 24 wherein said processor maps said technology independent RTL netlist to a selected technology architecture.

27. ~~24.~~ A digital processing system as in claim ~~23~~ 26 wherein said processor maps said technology independent RTL netlist after said processor performs said allocating.

28. ~~25.~~ A digital processing system as in claim ~~23~~ 26 wherein said processor performs a place and route operation after said processor maps said technology independent RTL netlist, wherein said place and route operation creates a representation of circuitry in said selected technology architecture.

29. ~~26.~~ A digital processing system as in claim ~~24~~ 27 wherein said processor optimizes a design of said IC after said processor performs said allocating.

30. ~~27.~~ A digital processing system as in claim ~~25~~ 27 wherein said processor maps said technology independent RTL netlist after said processor performs said allocating.

31. ~~28.~~ A digital processing system as in claim ~~27~~ 30 wherein said processor maps portions of said technology independent RTL netlist to said selected technology

SCANNED

architecture to generate estimates of IC resources and wherein said processor maps said portions after said processor compiles said HDL code.

32. ~~29~~. A digital processing system as in claim ~~27~~ 30 wherein said processor displays said estimates on said display device and stores said estimates in said memory.

33. ~~30~~. A digital processing system as in claim ~~29~~ 32 wherein said processor displays graphical representations of the area of said IC on said display device and displays on said display device representations of portions of said technology independent RTL netlist and wherein said processor performs said allocating in response to a command from a user.

34. ~~31~~. A digital processing system as in claim ~~30~~ 33 wherein estimates of area requirements of said portions of said technology independent RTL netlist are displayed on said display device.

35. ~~32~~. A machine readable medium containing a plurality of executable instructions, which when executed on a digital processing system cause said digital processing system to perform a method for designing an integrated circuit (IC), said method comprising:

compiling an hardware description language (HDL) code to produce a technology independent RTL (register transfer level) netlist;

allocating a portion of an area of said IC to a specific portion of said technology independent RTL netlist.

36. ~~33~~. A machine readable medium as in claim 35 ~~32~~ wherein said allocating restricts circuitry created from said specific portion to said portion of said IC.

38. ~~34~~. A machine readable medium as in claim 35 ~~32~~, wherein said method further comprises:

mapping said technology independent RTL netlist to a selected technology architecture.

37. ~~35~~. A machine readable medium as in claim 38 ~~34~~ wherein said IC comprises one of a programmable logic device or an ASIC.

40. ~~36~~. A machine readable medium as in claim 38 ~~34~~ wherein said mapping is performed after said allocating.

41. ~~37~~. A machine readable medium as in claim 38 ~~34~~, said method further comprising:

performing a place and route operation after said mapping to implement said IC in said selected technology architecture.

44. ~~38~~. A machine readable medium as in claim 38 ~~34~~, said method further comprising:

optimizing a design of said IC after said allocating.

45. 44
~~39~~. A machine readable medium as in claim ~~38~~ wherein said optimizing optimizes said IC by removing duplicative logic or input/outputs.

42. 38
~~40~~. A machine readable medium as in claim ~~34~~ wherein said HDL code is created without regard to said allocating.

46. 44
~~41~~. A machine readable medium as in claim ~~38~~ wherein said optimizing and said mapping are performed after said allocating.

52. 38
~~42~~. A machine readable medium as in claim ~~34~~, said method further comprising:
mapping portions of said technology independent RTL netlist to a selected technology architecture wherein estimates of IC resources are obtained from said mapping portions and wherein said mapping portions is performed after said compiling and before said mapping.

38
43. A machine readable medium as in claim ~~34~~, said method further comprising:
optimizing interconnects between modules of said technology independent RTL netlist before said allocating.

53. 52
~~44~~. A machine readable medium as in claim ~~42~~ wherein said estimates are used to decide how to perform said allocating.

SCANNED

54. 45. A machine readable medium as in claim 44 53 wherein a user considers said estimates and selects a command to decide how to perform said allocating.

51. 46. A machine readable medium as in claim 34 38 wherein said IC comprises a programmable logic device and wherein said method further comprises:

testing a prototype of a system with said IC;

performing a synthesis of said HDL code to generate at least one Application Specific Integrated Circuit (ASIC).

47. A machine readable medium as in claim 34 38, said method further comprising:

partitioning said technology independent RTL netlist between representations of said IC and another IC.

48. A machine readable medium as in claim 47 wherein said partitioning is performed before said mapping.

49. A machine readable medium as in claim 47, said method further comprising:

selecting logic designed for placement on one of said IC and said another IC and replicating said logic for placement on the other of said IC and said another IC.

50. A machine readable medium as in claim 47, said method further comprising:

selecting one RTL component in said technology independent RTL netlist and splitting said one RTL component into a first RTL component designed for placement on said IC and a second RTL component designed for placement on said another IC.

55. ~~51.~~ A system for designing an integrated circuit (IC), said system comprising:

means for compiling a hardware description language (HDL) code to produce a technology independent RTL (register transfer level) netlist;

means for allocating a portion of an area of said IC to a specific portion of said technology independent RTL netlist.

56. ~~52.~~ A system as in claim 55 ~~51~~ wherein said allocating restricts circuitry created from said specific portion to said portion of said IC.

57 ~~53.~~ A system as in claim 55 ~~51~~ further comprising:

means for mapping said technology in dependent RTL netlist to a selected technology architecture.

58. ~~54.~~ A system as in claim 57 ~~53~~ wherein said IC comprises one of a programmable logic device or an ASIC.

59. ~~55.~~ A system as in claim 57 ~~53~~ wherein said mapping is performed after said allocating.

60. ~~56.~~ A system as in claim 57 ~~53~~ further comprising:

means for performing a place and route operation after said mapping to implement said IC in said selected technology architecture.

71. ~~57.~~ A system as in claim 57 ~~53~~ further comprising:

means for optimizing a design of said IC after said allocating.

72. ~~58.~~ A system as in claim 71 ~~57~~ wherein said optimizing optimizes said IC by removing duplicative logic or input/outputs.

61. ~~59.~~ A system as in claim 57 ~~53~~ wherein said HDL code is created without regard to said allocating.

73. ~~60.~~ A system as in claim 71 ~~57~~ wherein said optimizing and said mapping are performed after said allocating.

62. ~~61.~~ A system as in claim 57 ~~53~~ further comprising:

means for mapping portions of said technology independent RTL netlist to a selected technology architecture wherein estimates of IC resources are obtained from said mapping portions and wherein said mapping portions is performed after said compiling and before said mapping.

SCANNED

62. 10. 57 A system as in claim 58 further comprising:

means for optimizing interconnects between modules of said technology independent RTL netlist before said allocating.

63. 62 A system as in claim 61 wherein said estimates are used to decide how to perform said allocating.

64. A system as in claim 63 wherein a user considers said estimates and selects a command to decide how to perform said allocating.

65. 57 A system as in claim 58 wherein said IC comprises a programmable logic device and wherein said system further comprises:

means for testing a prototype of a system with said IC;

means for performing a synthesis of said HDL code to generate at least one Application Specific Integrated Circuit (ASIC).

66. 57 A system as in claim 58 further comprising:

means for partitioning said technology independent RTL netlist between representations of said IC and another IC.

67. A system as in claim 66 wherein said partitioning is performed before said mapping.

68. A system as in claim 66 further comprising:

means for selecting logic designed for placement on one of said IC and said another IC and replicating said logic for placement on the other of said IC and said another IC.

69. A system as in claim 66 further comprising:

means for selecting one RTL component in said technology independent RTL netlist and splitting said one RTL component into a first RTL component designed for placement on said IC and a second RTL component designed for placement on said another IC.

20
~~70.~~ A method as in claim 1 further comprising:

selecting logic designed for placement in one of said area of said IC and another area of said IC and replicating said logic for placement on the other of said area and said another area.

37.
~~71.~~ A machine readable medium as in claim ~~32~~ 35, said method further comprising:

selecting logic designed for placement in one of said area of said IC and another area of said IC and replicating said logic for placement on the other of said area and said another area.

~~72.~~ A method as in claim 1 further comprising:

21.

selecting one RTL component in said technology independent RTL netlist and splitting said one RTL component into a first RTL component designed for placement in said area of said IC and a second RTL component designed for placement in another area of said IC.

22. ~~13~~. A machine readable medium as in claim 21 ~~12~~, said method further comprising:

selecting one RTL component in said technology independent RTL netlist and splitting said one RTL component into a first RTL component designed for placement in said area of said IC and a second RTL component designed for placement in another area of said IC.

SCANNED